

What is claimed is:

1. A semiconductor device, comprising:

5 a plurality of capacitor plugs formed within a predetermined interval interleaved between two bit lines and midpoints of capacitor plugs are located at intersection points of X axis virtual line and Y axis virtual line, wherein the X axis virtual lines are parallel with the bit lines and the Y axis virtual lines are vertical to the X axis virtual lines; and

10 a plurality of lower electrodes of capacitors formed within a predetermined interval to be respectively connected with the capacitor plugs in one to one correspondence,

15 each lower electrode being octagonally or circularly shaped.

2. The semiconductor device as recited in claim 1, wherein a lower electrode and neighbored lower electrode in a direction of Y virtual axis line are formed 20 not to have overlapped area, if one of lower electrode is moved to same X virtual axis line as the other lower electrode.

3. The semiconductor device as recited in 25 claim 1, wherein the lower electrode and neighbored lower electrode in a direction of Y virtual axis are not on the same Y virtual axis.

4. The semiconductor device as recited in 30 claim 1, wherein the midpoints of the lower electrode and the neighbored lower electrode are not on the same Y virtual axis.

5. The semiconductor device as recited in  
claim 1, wherein a ratio of a major axis to a minor axis of  
the upper plane of the lower electrodes ranges from about 1  
5 to 1 to about 2 to 1.

6. The semiconductor device as recited in  
claim 1, wherein an area of an upper plane of the lower  
electrode is practically identical to that of an lower  
10 plane of the lower electrode in view of a three-dimensional  
structure and the lower electrode features a octagonal or a  
circular cylinder structure having a lateral plane  
connecting the upper plane with the lower plane, wherein  
the lateral plane is substantially vertical to the upper  
15 plane and lower plane respectively.

7. The semiconductor device as recited in  
claim 1, wherein a plurality of contact pads are formed  
between the lower electrodes and the capacitor plugs,  
20 wherein the contact pads are formed over the capacitor  
plugs and disposed at a lower plane of at least one of the  
paired lower electrodes.

8. The semiconductor device as recited in  
25 claim 7, wherein a midpoint of the contact pad is located  
at an upper plane of the capacitor plug along one of two X  
virtual axes which is adjacent to each other.

9. The semiconductor device as recited in  
30 claim 8, wherein a midpoint of the contact pad is deviated  
from the midpoint of a corresponding capacitor plug but  
located at a midpoint of the corresponding lower electrode.

10. The semiconductor device as recited in  
claim 8, wherein a midpoint of the contact pad is located  
at a midpoint of the corresponding lower electrode and the  
5 lower electrode corresponding to the contact pad and  
another lower electrode which is adjacent to the lower  
electrode corresponding to the contact pad along the Y  
virtual axis are disposed at positions deviated from the Y  
virtual axis in an opposite direction.

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11. The semiconductor device as recited in  
claim 8, wherein size of the upper plane of the contact pad  
is greater than that of the upper plane of the capacitor  
plug.

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12. A method for fabricating a semiconductor  
device, comprising:

20 a) forming a plurality of capacitor plugs within  
a predetermined interval interleaved between two bit lines  
by arranging midpoints of capacitor plugs located at inter-  
section points of X axis virtual line and Y axis virtual  
line, wherein the X axis virtual lines are parallel with  
the bit lines and the Y axis virtual lines are vertical to  
the X axis virtual lines; and

25 b) forming a plurality of lower electrodes of  
capacitors within a predetermined interval to be  
respectively connected with the capacitor plugs in one to  
one correspondence, each lower electrode being octagonally  
or circularly shaped.

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13. The method as recited in claim 12, wherein  
part step b) further comprises:

b-1) depositing a sacrifice insulation layer over  
the capacitor plug formed over a semiconductor substrate;

5 b-2) forming a plurality of open parts exposing  
the capacitor plugs by performing an selective etching of  
the sacrifice insulation layer by using a mask pattern;

b-3) depositing a material for the lower  
electrode on an entire profile of the semiconductor  
10 substrate comprising the open parts;

b-4) forming the lower electrodes separated from  
each other by performing a planerization process until the  
sacrifice insulation layer is exposed; and

b-5) removing the sacrifice insulation layer by  
15 carrying out a wet dip-out process.

14. The method as recited in claim 13, wherein  
the mask pattern having an open part and neighbored open  
part in a direction of the Y virtual axis line are formed  
20 not to have overlapped area or to have minimum overlapped  
area, if the open part is moved to the same X virtual axis  
line as the other open part.

15. The method as recited in claim 14, wherein  
25 the mask pattern having the open part and neighbored open  
part in a direction of the Y virtual axis are not on the  
same Y virtual axis.

16. The method as recited in claim 14, wherein  
30 the mask pattern having the open part and the neighbored  
open part are not on the same Y virtual axis.

17. The method as recited in claim 14, wherein  
the open part of the mask pattern features an octagonal or  
a circular shape and a ratio of a major axis to a minor  
axis of the open part ranges from about 1 to 1 to about 2  
5 to 1.

18. The method as recited in claim 12, wherein  
an area of an upper plane of the lower electrode is  
practically identical to that of an lower plane of the  
10 lower electrode and the lower electrode has an octagonal or  
circular cylinder structure which has a lateral plane  
connecting the upper plane with the lower plane and  
practically vertical to the upper plane and lower plane.

15 19. The method as recited in claim 12, wherein  
a plurality of contact pads are respectively formed between  
the lower electrodes and the capacitor plugs after forming  
the capacitor plugs, wherein the contact pads serve as  
connecting the lower electrode with the capacitor plug  
20 electrically.

20. The method as recited in claim 19, wherein  
the contact pads are formed over the capacitor plugs and  
midpoints of the contact pads are located at a lower plane  
25 of at least one of the paired lower electrodes along the X  
virtual axis.

21. The method as recited in claim 19, wherein  
the contact pads are disposed on upper planes of the  
30 capacitor plugs of which midpoints are located along one of  
a pair of X virtual axes adjacent to each other.

22. The method as recited in claim 20, wherein the midpoints of the contact pads are deviated from the midpoints of corresponding capacitor plugs and respectively located at midpoints of corresponding lower electrodes.

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23. The method as recited in claim 20, wherein a midpoint of the contact pad is located at a midpoint of the corresponding lower electrode and the lower electrode corresponding to the contact pad and an adjacent lower electrode found along the Y virtual axis are disposed in a way crossing each other.

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15 24. The method as recited in claim 20, wherein size of the upper plane of the contact pad is greater than that of the upper plane of the capacitor plug.